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IMAGE PROCESSING SYSTEM FOR SEMICONDUCTOR CHIP COUNTING AT PT ELEKTRONIK INDONESIA

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Abstract: Conventional semiconductor chip counting at PT Elektronik Indonesia relies on manual weighing, which is prone to human error and inefficiency. This study proposes a desktop-based counting system using a digital scanner and image processing. The novelty lies in integrating horizontal-vertical projection with probabilistic Hough transform to robustly detect grid lines, form square cells, and enable accurate unit estimation via average intensity analysis, eliminating the need for reference weighing. Experiments on 15 actual chip images yielded an error rate of 0.009519% and up to 73.674%time efficiency gains compared to the manual method. The system reduces operator dependency, minimizes errors, and accelerates counting, providing a practical machine vision solution for semiconductor production.

Keywords: chip counting; image processing; probabilistic hough transform; grid line detection; time effeciency.

Abstrak: Penghitungan chip semikonduktor konvensional di PT Elektronik Indonesia bergantung pada penimbangan manual, yang rentan terhadap kesalahan manusia dan kurang efisien. Penelitian ini mengusulkan sistem penghitungan berbasis desktop menggunakan scanner digital dan pengolahan citra. Kebaruan terletak pada integrasi proyeksi horizontal-vertikal dengan probabilistic Hough transform untuk mendeteksi garis grid secara kuat, membentuk sel persegi, serta memungkinkan estimasi unit akurat melalui analisis intensitas rata-rata, sehingga menghilangkan kebutuhan penimbangan referensi. Eksperimen pada 15 citra chip aktual menghasilkan tingkat kesalahan 0,009519% dan peningkatan efisiensi waktu hingga 73,674% dibandingkan metode manual. Sistem ini mengurangi ketergantungan operator, meminimalkan kesalahan, dan mempercepat penghitungan, menyediakan solusi machine vision praktis untuk produksi semikonduktor.

Kata kunci: penghitungan chip; pengolahan citra; probabilistic Hough transform; deteksi garis grid; efisiensi waktu.

INTRODUCTION

Modern semiconductor manufactu ring requires precise component counting, yet PT Elektronik Indonesia still relies on manual weighing of 500 chip samples, a method prone to human error, weight variations, and fatigue-induced inaccuracies. While Industry 4.0 technologies like computer vision have transformed industrial automation [1], [2]. Existing semiconductor research focuses primarily on defect inspection rather than counting solutions [3], [4], [5]. Although image-based counting has succeeded in agriculture and aquaculture [6], [7], [8], the semiconductor sector lacks practical,

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cost-effective systems for high-density chip counting using accessible hardware like standard scanners.

This study develops an automated counting system to replace manual weighing at PT Elektronik Indonesia through a desktop application integrating digital scanners with real-time image processing. Unlike expensive optical setups, this system solution employs fundamental image analysis techniques by using grid segmentation and object intensity evaluation [9]. The noveltiy relies on hybrid approach combines horizontal-vertical image projection with probabilistic Hough transform [10] to detect structural grid patterns from scanned images, enabling accurate chip quantification without manual reference.

The system's breakthrough lies in its robust grid pattern detection through integrated projection techniques and Hough transform analysis [11]. By analyzing average intensity distributions across segmented grids, it achieves counting accuracy comparable to manual methods while eliminating human error factors. This costeffective solution demonstrates how accessible scanning hardware coupled with intelligent algorithms can bridge the automation gap in semiconductor manufacturing workflows.

The implemented system aligns with Industry 4.0's digital transformation goals by demonstrating scalable machine vision adoption using existing infrastructure [12]. Beyond PT Elektronik Indonesia, it provides a blueprint for sensor-based automation in semiconductor manufacturing, promoting sustainable production through intelligent analytics. This research contributes to high-throughput electronic manufacturing by replacing unreliable manual processes with precise, data-driven counting methodologies.

METHOD

This study develops a digital image processing system integrated with hardware components, including a digital scanner, computer, and monitor. The scanner captures high-resolution semiconductor chip images, the computer processes them through acquisition, preprocessing, segmentation, and automatic counting, while the monitor displays results and real-time chip counts via a user interface. Fig. 1 illustrates the system's data flow from scanner to computer for processing and visualization.

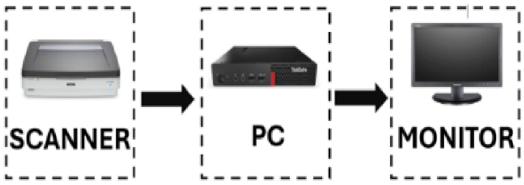

Figure 1.Hardware Design.

The system is implemented as a desktop application featuring a GUI connected to a digital scanner, with three key components: an input image displaying the scanned chip layout for operator verification, a processed image showing segmentation results to confirm detection accuracy, and a results table providing regional and total chip counts for production tracking and process evaluation. This design follows standard practices for automated counting systems, with the complete workflow illustrated in Figure 2.

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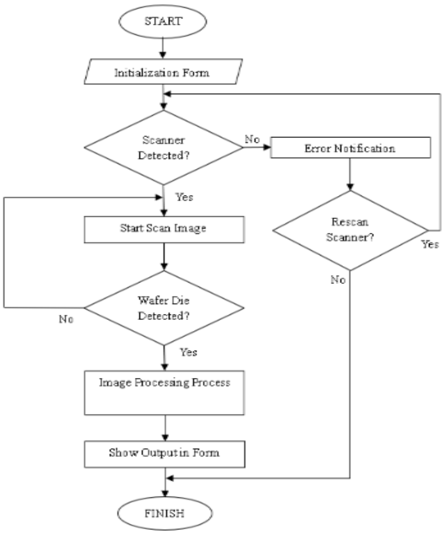

Figure 2.GUI Application Design.

The proposed method automatically detects and counts square-shaped semiconductor chips by combining preprocessing, Hough transform-based line detection, row column projection, and pixel intensity analysis. The process begins with Gaussian filtering to reduce noise, followed by grayscale conversion and binarization to separate objects from the background. Morphological dilation reinforces edges, and the probabilistic Hough transform identifies horizontal and vertical lines for grid formation as defined in formula formula (1). The horizontal $P_h(y)$ and vertical projections $P_v(x)$ are defined as the number of active pixels in each row and each column.

$$P_h(y) = \sum_{x=0}^{W-1} B(x,y), P_v(x) = \sum_{y=0}^{H-1} B(x,y) \quad (1)$$

where $B(x,y)$ denotes a binary image of size $W \times H$. The threshold value for detecting projection peaks is determined adaptively from the mean of the projection using formula (2).

$$T_h = \alpha_h \cdot \bar{P}_h, T_v = \alpha_v \cdot \bar{P}_v \quad (2)$$

The system uses paramete rs α_h and α_v represent the horizon tal_threshold and vertical_threshold to control line detection sensitivity. Projec tion peaks exceeding these thresholds are filtered by minimum inter-peak distance and merged with Hough detection lines, ensuring stable horizontal and vertical coordinates for imperfect grids[13]. Boundary lines are added for complete grid coverage, forming square cells Ω_{ij} each analyzed for mean intensity using formula (3).

$$\mu_{ij} = \frac{1}{|\Omega_{ij}|} \sum_{(x,y)\in\Omega_{ij}} G(x,y) \quad (3)$$

A cell Ω_{ij} is classified as a valid square if it satisfies the criterion given in formula (4).

$$\mu_{ij} > T_w \quad (4)$$

The parameter T_w is selected based on image characteristics and aligns with region-based intensity analysis methods used in automatic cell and particle counting systems. Cells meeting this criterion are annotated by drawing boxes on the output image, and the counter N_{chip} is incremented for each valid cell detected [14], [15]. Before grid construction, chip contours are extracted and filtered by size, enabling independent square detection per chip region. The final output accumulates valid squares across all regions, computing units per substrate and total counts for comparison with manual results. The pipeline Fig. 3 includes image acquisition, preprocess

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ing, grid formation, intensity analysis, and chip counting.

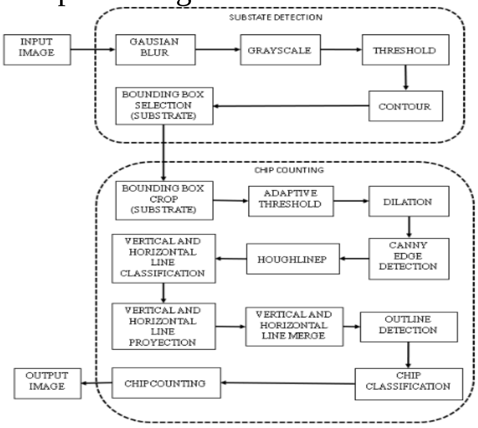

Figure 3.Image Processing Design

RESULT AND DISCUSSION

The semiconductor chip counting system has been successfully implemen ted and tested at PT Elektronik Indonesia, demonstrating greater efficiency and accuracy compared to manual methods. The system integrates with a digital scanner and features an intuitive GUI that displays the original scanned image, the processed image with detection markers, and a results table showing individual chip counts and total units in Fig. 4. Rigo rous testing under varying chip densities and lighting conditions confirmed high accuracy and significantly faster proce ssing times.

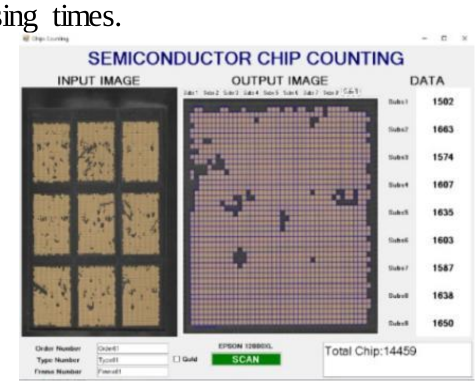

Figure 4.GUI Application

The process begins with preprocessing acquired RGB images to reduce noise and enhance segmentation. Images are smoothed using a Gaussian filter, converted to grayscale, and binarized through thresholding to separa te chip regions from the background as shown in Fig. 5.

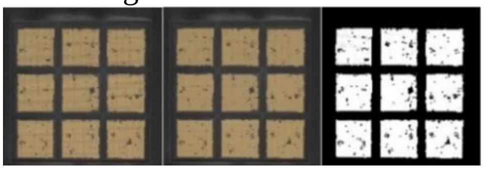

Figure 5.Substrate Detection Step

Contours are then extracted using cv2.findContours, and bounding boxes are computed for each contour. Only those meeting predefined size criteria are selected as candidate substrates in Fig. 6, which are subsequently sorted top-to-bottom and left-to-right for consistent indexing.

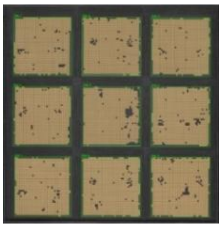

Figure 6.Substrate Detection

Each chip image is cropped individually, and adaptive thresholding THRESH_BINARY_INV is applied to produce a binary image with bright obje cts on a dark background. Morphological dilation reinforces grid lines as shown in Fig. 7, which compares the original chip image, the adaptive-threshold result, and the dilated image.

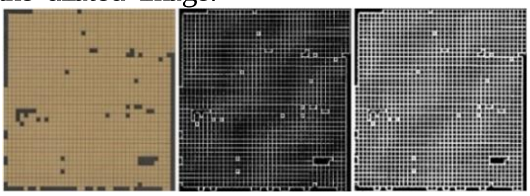

Figure 7.Dilation Step.

Grid lines are detected using a combination of probabilistic Hough trans form cv2.HoughLinesP and projection methods, yielding stable horizontal and vertical lines. The resulting grid visualization is presented in Fig. 8, where horizontal lines are drawn in green and vertical lines in red on the chip image.

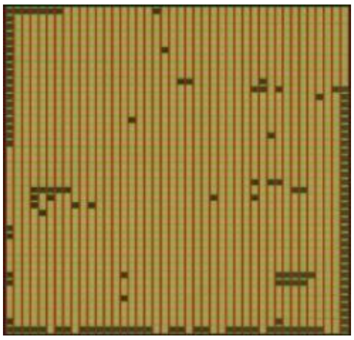

Figure 8.Merge Vertical and Horizontal Line Steps

The chip area is partitioned into square cells defined by adjacent line pairs. Mean pixel intensity is computed for each cell, and only those exceeding the threshold are classified as valid squares. Valid squares are annotated and counted, with results displayed shown in Fig. 9 numerically and visually.

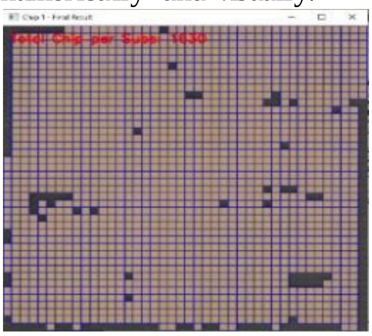

Figure 9.Chip Counting Result

Quantitatively, the system performance compared with the manual method used by the company is summarized in Table 1. The table lists the number of units obtained by manual counting and by the system for several chip samples. Based on the available test data, the average system error percentage is 0.009519%, indicating that the difference between the system's counting results and the manual method is very small. These findings demonstrate that the implemented image processing algorithm can accurately represent the number of units on the chips under image conditions that meet the design specifications.

Table 1. Different Chip Count

Nr.	Manual Count	System Count	Error(%)
1	14463	14459	0,027657
2	16585	16582	0,018089
3	14844	14843	0,006737
4	10473	10473	0
5	12866	12865	0,007772
6	9456	9456	0
7	10458	10459	0,009562
8	15920	15921	0,006281
9	13680	13679	0,00731
10	9536	9537	0,010487
11	18930	18932	0,010565
12	11876	11875	0,00842
13	14575	14578	0,020583
14	10722	10721	0,009327
15	16054	16054	0

To assess the practical benefits of the system, a processing time performance comparison was carried out between the weighing based manual method and the automatic image processing-based method. In this evaluation, several chip quantity scenar-ios were tested, and Table 2 reports the average time required to complete the counting process using both the manual method and the proposed system, togeth-er with the corresponding time saving percentage.

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Table 2. Different Counting Process Time

Nr.	Manual Time (minute)	System Time (minute)	Time Efficiency (%)
1	11	3	72,72727
2	12	3	75
3	11	3	72,72727
4	10	3	70
5	12	3	75
6	10	3	70
7	12	3	75
8	12	3	75
9	12	3	75
10	10	3	70
11	12	3	75
12	11	3	72,72727
13	12	3	75
14	12	3	75
15	13	3	76,92308

The performance of the image processing algorithm was evaluated by analyzing the impact of parameter variations and image conditions on detection results. Key parameters include horizontal_threshold and vertical_threshold, which control line detection sensitivity, min_line_distance for grid stability, and chip_threshold for classifying valid squares. Through experiments, Table 3 identifies the optimal parameter combination, balancing sensitivity and noise robustness.

Table 3. System Parameter

Parameter	Value
horizontal_threshold	1
vertical_threshold	1
Min_line_distance	10
chip_threshold	130

The system performs well on images with consistent scanning quality, sufficient contrast, and neat chip arrangements. Techniques like Gaussian blur, binary thresholding, and dilation reduce noise and reconnect broken lines, while Hough transforms and line projection enhance robustness. At PT Elektronik Indonesia, the system reduces manual dependence, improves consistency, and integrates seamlessly into workflows, boosting production efficiency. However, it relies heavily on scanning consistency and is tailored to specific grid patterns, requiring adjustments for design changes. Future improvements include integration with manufacturing systems.

CONCLUSION

Semiconductor chip counting system using image processing successfully replaces the manual weighing method at PT Elektronik Indonesia, achieving an error rate of 0.009519% and up to 73.674%time efficiency improvement (from ~11 minutes to 3 minutes per 13,000 chip batch). Integration of a digital scanner, computer, and GUI provides an intuitive workflow with real-time visualization of processing and counting results. The hybrid algorithm combining horizontal–vertical projection, Hough transform, and average intensity analysis of square cells proved effective for NTC thermistor chip detection and counting across 15 test images under standard 1200 dpi scanning conditions with 13,000 chips per image.

The system reduces operator workload, minimizes human error, and enhances production throughput. This research supports digital transformation and Industry 4.0 initiatives in domestic electronic manufacturing. Future developments include algorithm robustness against extreme image variations, machine learning integration, real-time industrial cameras, and connectivity with large scale production systems.

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